

AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Please replace the paragraph beginning on page 5, line 3, with the following rewritten paragraph:

--Refer to Fig. 2 and Fig. 8. In DE mode, the ~~vertical~~  
~~synchronizing signal generated from decoding the signal DE, instead~~  
~~of the vertical blank period VB (v-blank) and gate clock signal~~  
~~CPV, is~~ are used as a reference basis in the prior art. Signals  
~~are processed at the rising edge or the falling edge of a~~ In the  
present invention, the vertical synchronizing signal, and the  
control signals of the LCD module 10 are generated from decoding  
the signal DE is used as a reference basis. At the rising edge or  
the falling edge of the vertical synchronizing signal, signals are  
processed to generate the control signals of the LCD module 10 in  
real time. For example, after the start vertical signals STV1, STV2  
and the gate-on enable signal OE are generated in real time, the  
CPV (gate clock signal), STV1, STV2, and OE pause to be outputted  
till the timing controller 12 detects a first DE signal after the  
vertical blanking period, and then the normal control signals  
restart to be outputted so that the real time driving is  
achieved.--

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